

Code No: **R204104S**

R20

SET - 1

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM

IV B. Tech I Semester Regular/Supplementary Examinations OCT/NOV 2025

IC APPLICATIONS

(OPEN ELECTIVE)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**

All Questions Carry Equal Marks

UNIT-I

1. a) Design an inverting and non-inverting amplifiers using Op Amp and then [7M]
derive their voltage gain expressions.
b) Explain the DC and AC characteristics of an Op-Amp. [7M]
(OR)
2. a) Construct an Op-Amp based square wave generator and then explain its [7M]
operation.
b) Design an Op Amp based active LPF and HPF and then explains their working. [7M]

UNIT-II

3. a) Draw the functional block diagram of IC 555 and then explain the function of [7M]
each block.
b) Describe the monostable operation of 555 timer and derive its pulse width [7M]
expression.
(OR)
4. a) Describe the concept of Phase-Locked Loop (PLL) and its basic building [7M]
blocks.
b) Explain the astable operation of 555 timer and then derive its frequency and [7M]
duty cycle expressions.

UNIT-III

5. a) Draw and explain the circuit of a 4-bit weighted resistor DAC and then derive [7M]
its output expression.
b) Design a 4-bit R-2R ladder DAC and then calculate its output voltage for a [7M]
1010 binary input. Assume 5V supply.
(OR)
6. a) Discuss the working of 4-bit successive approximation ADC with one example. [7M]
b) List and explain some of the important ADC and DAC specifications. [7M]

UNIT-IV

7. a) Design a BCD-to-seven-segment decoder using standard TTL ICs. [7M]
b) Design an 8X1 multiplexer and then explain how it can implement Boolean functions with one example. [7M]

(OR)

8. a) Design a 4-bit parallel binary adder/subtractor circuit using IC 7483 and explain its operation. [7M]
b) Explain the operation of an 8-to-3 priority encoder using truth table and logic diagram. [7M]

UNIT-V

9. a) Describe the operation of SR, JK, D, and T flip-flops with logic diagrams and truth tables. [7M]
b) Explain the conversion of a JK flip flop to D Flip flop in detail? [7M]
- (OR)
10. a) Draw and explain the working of universal shift register (IC 7495 or 74194). [7M]
b) Design a 4-bit synchronous up/down counter using JK flip-flops and explain its operation. [7M]
